Hashem Hashemi Najaf-abadi

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Education

PHD Candidate in Computer Eng., NC State University, since 2005
MSc in Computer Architecture, Sharif Univ. of Tech., Tehran, 2002-2004
BS in Computer Hardware, IAUCTB, Tehran, 1997-2002

Research Experience

Research Intern, Intel., Hudson, MA, July-Oct. 2010:

- *Research on the interaction between smart cache replacement policies and task placement policies in multi-cluster CMPs.*

Research Intern, Qualcomm Inc., NC, Feb-Aug 2008:

- *Modeling the power and AXI bus performance of the Scorpion processor with available event counters. Measurements were made on development boards.*

Research Assistant, ECE Department, NC State University, since Aug. 2005:

- *Computer architecture. Heterogeneous microarchitectures. Specifically, understanding the influence of workload behavior on the design of pipelined processors in the presence of circuit-level tradeoffs between propagation delay and complexity.*

Research Assistant, School of Computer Science, Institute for studies in theoretical Physics and Mathematics (IPM), Tehran, 2003-2005:

- *Performance modeling and evaluation of interconnection networks.*

Research Intern, Iranian Research Org. for Science & Technology, Tehran, 2001-2002:

- *Complete logic, schematic and PCB design, programming and debugging of a chemical fermentation system based on the i80196 microprocessor.*

Refereed Publications

H. H. Najaf-abadi, E. Rotenberg, "The Importance of Accurate Task Arrival Characterization in the Design of Processing Cores", I*n Proc. of the IEEE International Symposium on Workload Characterization (IISWC)*, 2009.

H. H. Najaf-abadi, N. K. Choudhary, E. Rotenberg, "Core-Selectability in Chip Multiprocessors", I*n Proc. of the Conference on Parallel Architectures and Compilation Techniques (PACT)*, 2009.

H. H. Najaf-abadi, E. Rotenberg, "Architectural Contesting", In *Proc. of the International Symposium on High-Performance Computer Architecture (HPCA)*, 2009.

H. H. Najaf-abadi, E. Rotenberg, "Configurational Workload Characterization", In *Proc. of the International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2008.

H. H. Najaf-abadi, E. Rotenberg, "Exploiting Detachability: A Non-Silicon Approach to Polymorphism", *the Non-Silicon Computing Workshop (in conjunction with ISCA-34)*, 2007.

H. H. Najaf-abadi, H. Sarbazi-azad, "Mathematical Performance Modeling of Adaptive Wormhole Routing in Optoelectronic Hypercubes", In *Journal of Parallel and Distr. Computing (JPDC)*, 2007.

H. H. Najaf-abadi, H. Sarbazi-azad, "An accurate combinatorial model for performance prediction of deterministic wormhole routing in torus multicomputer systems", In *Proceedings of the International Conference on Computer Design (ICCD)*, 2004, USA.

H. H. Najaf-abadi, "A procedure for obtaining a behavioral description for the control logic of a non-linear pipeline", In *Proceedings of the Asia & South Pacific Design Automation Conference (ASP-DAC)*, 2004.

see webpage for complete list

Book chapters

H. H. Najaf-abadi, H. Sarbazi-azad, "Performance Modeling of Optoelectronic OTIS Cubes", Performance Evaluation of Parallel and Distributed Systems, Distributed, Cluster and Grid Computing, Vol. 1, Nova Science, 2005.

Teaching Experience

Lecturer for complete course on Advanced Microprocessors,
Iran University of Science and Technology, Tehran (fall 2004)

- *The text book I used was: J. Silc, B. Robic, T. Ungerer, "Processor Architecture, from Dataflow to Superscalar and Beyond", Springer-Verlag 1999.*

Conductor of Computer Architecture Lab,
Sharif University of Technology, Tehran (Fall & Spring 2003)

- *I developed a set of well-defined examples for students to gradually implement a simple non-pipelined processor using TTL gates. The final implementation would sequence through code (in dedicated static RAM), and perform basic operations with self-defined opcodes. This provided students with a glimpse at intricacies that are not conveyed in architecture-level courses.*

Relevant Course Work

- Code Generation and Optimization ECE566 (final grade: A+)
  Course project: implementation of a simple C compiler implementing register allocation, dead code elimination, and constant/copy propagation.
- Digital ASIC Design ECE520 (final grade: A)
  Course project: Verilog implementation of the back-end of a speech recognition system.
- Memory Systems ECE705 (final grade: A)
  Course project: comparing the performance interaction between prefetching and value prediction (implemented in the GEMS simulator).
- Advanced Microarchitecture ECE721 (final grade: A)
  Course project: implementation of checkpoint processing and recovery (CPR).

Personal

US Visa Status: F1
Citizenship: Australian (dual national)

References

Dr. Eric Rotenberg	ericro@ece.ncsu.edu	(919) 513-2822
Dr. Tom Conte	conte@cc.gatech.edu	(404) 385-7657
Dr. Greg Byrd	gbyrd@ece.ncsu.edu	(919) 513-2508

other references available on request